Attorney Docket No.: N1280-00120(TSMC2003-0919

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name; and

I verily believe that I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled OUTPUT BUFFER ESD PROTECTION USING PARASITIC SCR PROTECTION CIRCUIT FOR CMOS VLSI INTEGRATED CIRCUITS, the specification of which:

L	j	18 attached her	eio.		•
[[]	was filed on and was amend	ded on	as Applic	ation Serial No (If applicable.)
I hereby specifica	state	that I have revi including the cl	ewed and unde aims, as amen	erstand the cont ded by any Am	ents of the above-identified endment referred to above.
applicati	ion in	accordance wit	h 37 C.F.R. §	1.56.	aterial to the patentability of this
patent of applicati	r invertion for	ator's certificate	listed helow:	and have also 10	119 of any foreign application(s) for dentified below any foreign ag date before that of any application
Country	:		Number	Date <u>Filed</u>	Priority <u>Claimed</u>
î	N/A				
		by claim the best ted below:	nefit under 35	U.S.C. § 119(e)	of any United States provisional
<u>Applica</u>	tion			<u>Filed</u>	
N/A					
				1	·
TSMC2003	-0919 D	eclaration and Power o	f Attorney	•	

I hereby appoint the following attorneys, of the law firm DUANE MORRIS LLP, One Market Street, Spear Tower, Suite 2000, San Francisco, CA 94105-1104, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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